IN THE CLAIMS

Claim 29 has been amended as follows:

(AMENDED TWICE) A stacked-gate flash memory having a shallow trench isolation with a high-step oxide and high lateral coupling comprising:

a substrate having a gate oxide layer;

at least two trenches formed to a depth between about 2500 to 5000 Å below the surface of said substrate;

an oxide [liner] <u>layer</u> formed over said substrate, including over the inside walls of said two trenches;

a high-step oxide formed within said two trenches over said oxide liner and protruding upward over the surface of said substrate to a height between about 2000 to 6000 Å;

said high-step oxide forming an opening with high walls over the surface of said substrate between said two trenches;

a first [polysilicon] conductive layer formed conformally inside said opening and over the surface of the substrate between said high walls to form a floating gate having folding surfaces;

an intergate oxide formed over said floating gate having folding surfaces;

a second [polysilicon] conductive layer formed protruding downward in between said folding surfaces over said intergate oxide layer to form a control gate; and

a self-aligned source (SAS) line.